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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/010,161	11/13/2001	Brian C. Barnes	2000.056700	7264

23720 7590 11/15/2005

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EXAMINER	
ABYANEH, ALI S	
ART UNIT	**PAPER NUMBER**
2137	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/010,161	BARNES ET AL.	
	Examiner	Art Unit	
	Ali S. Abyaneh	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/6/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-37 are pending.

Information Disclosure Statement PTO-1449

2. The Information Discloser Statement submitted by applicant on 04-06-2005 has been considered. Please see attached PTO-1449.

3. Examiner withdraws objection to the abstract due to correction by the applicant.

4. Applicant indicated that a terminal disclaimer has been submitted. However, examiner is unable to locate the terminal disclaimer. Therefor double patenting rejecting stands as pervious office action.

Response to Arguments

5. Applicant's arguments filed 07-29-2005 have been fully considered but they are not persuasive.

Applicant contends that Maruyma does not teach, **"using a linear address to access at leas one security attribute data structure located in a memory to obtain a security attribute of a selected memory page in the memory"**. Examiner respectfully disagrees. Maruyma clearly discloses accessing a lookup table and comparing a master ID with the entries in the

lookup table, which corresponds to applicant's claim limitation (see column 6, lines 47-55). Maruyma furthermore teaches the master ID table (security attribute data structure) located on the memory unit (see column 5, lines 7-11). Therefore Maruyma teaches accessing security attribute data structure located in the memory to obtain a security attribute of a selected memory page in the memory.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1,11-13, 23, 32 and 36-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Teruyuki Maruyama et al. (US Patent NO.6,052,763).

Regarding Claims 1, 11-13, 23, 32 and 36-37

Maruyama teaches a processing unit 340 (execution unit) coupled to the memory unit 10 through the use of bus 15 and a memory controller 20 (memory management unit) coupled to the DRAM memory 19 (column 4, lines 62-67, column 6, lines 1-19 and fig 4). Maruyama furthermore teaches a memory management unit for managing a memory storing data arranged within a plurality of memory pages, the memory management

unit comprising: a security check unit (register 21) coupled to receive a linear address generated during execution of a current instruction (column 5, line 20-21), wherein the linear address has a corresponding physical address residing within a selected memory page [(column 5, line 23-24) (access address is accessing a range within DRAM 19. DRAM 19 has to be addressed by physical address)], and wherein the security check unit is configured to use the linear address to access at least one security attribute (processor master ID) data structure located in the memory to obtain a security attribute of the selected memory page, to compare a numerical value conveyed by a security attribute of the current instruction to a numerical value conveyed by the security attribute of the selected memory page, and to produce an output signal dependent upon a result of the comparison, if the processor master ID does not match, the comparator outputs a signal indicating an error (fault signal); if there is a match a different signal is outputted [(access addresses are stored in the decoder and master ID is sent to register 22. A comparator 23 is used to compare the master ID from the system bus with the bus master ID and outputs a signal)(column 6, lines 11-40 and column 5 lines 20-40)]; and wherein the memory management unit is configured to access the selected memory page dependent upon the output signal (column 6 lines 29-40). (Having a paging unit is inherent in the art in order to translate linear addresses to physical addresses).

Regarding Claims 2, 14, 21, 24 and 29

Maruyama teaches all limitation of the claim as applied to claim 1, 13 and 23 above and furthermore he teaches a master ID data structure 24 comprising a master ID table (table directory) and a lookup table (security attribute table) (column 6, lines 48-54).

Regarding Claims 3, 15 and 30

Maruyama teaches all limitation of the claim as applied to claim 2, 14 and 29 above and furthermore he teaches a memory controller 20 (memory management unit), wherein the master ID table (security attribute table directory) comprises a plurality of entries, and where each entry of the security attribute table directory includes a present bit and a security attribute table base address field, and wherein the present bit indicates whether or not a security attribute table corresponding to the security attribute table directory entry is present in the memory, and wherein the security attribute table base address field is reserved for a base address of the security attribute table corresponding to the security attribute table directory entry (column 6, lines 30-55 and fig 4).

Regarding Claims 4-6, 16-18, 27, 28 and 31

Maruyama teaches all limitation of the claim as applied to claims 2, 1, 14, 13, 23 and 29 above and furthermore he teaches using a master ID table (accessing one security attribute data structure) to extract a

master ID (obtain additional security attribute, SCID) and compare it to master ID of the accessing processor. The master IDs are indicators of security level of accessing processor since they determine if the processor is authorized to perform any transactions in the memory system (column 6, lines 30-55 and fig 4).

Regarding Claim 7

Maruyama teaches all limitation of the claim as applied to claims 1, above and furthermore he teaches a memory management unit, wherein the comparator (security check logic) is configured to obtain the master ID (security attribute) of the current instruction from the at least one master ID table (security attribute data structure) (column 6, lines 29-40 and fig 4).

Regarding Claim 8

Maruyama teaches all limitation of the claim as applied to claims 1, above and furthermore he teaches a memory management unit, wherein the output signal is a fault signal [(column 6, lines 35-40) (if the processor master ID does not match, the comparator outputs a signal indicating an error (fault signal); if there is a match a different signal is outputted)].

Regarding Claim 9

Maruyama teaches all limitation of the claim as applied to claims 1, above and furthermore he teaches a memory management unit, wherein

the register 21 (security check unit) is configured to receive a set of processor master ID (security attributes) of the selected memory page in addition to the master ID (security attribute) of selected memory page, and to produce the output signal dependent upon: (i) the result of the comparison of the numerical value conveyed by the master ID (security attribute) of the current instruction to the numerical value conveyed by the master ID (security attribute) of selected memory page, and (ii) the set of master ID (security attributes) of the selected memory page (column 6, lines 11-40).

Regarding Claims 19, 25 and 33

Maruyama teaches all limitation of the claim as applied to claims 13, 23 and 32 above and furthermore he teaches a memory controller 20 (memory management unit), wherein the register unit 21 (security check unit) is coupled to receive a current privilege level (CPL) of a current task including the current instruction, and configured to produce the output signal dependent upon: (i) the result of the comparison of the numerical values conveyed by the security attribute of the current instruction and the security attribute of selected memory page, and (ii) the CPL of the current task including the current instruction (column 6, lines 11-40 and fig 4).

Regarding Claim 34

Maruyama teaches all limitation of the claim as applied to claim 32 above and furthermore he teaches using an access address to obtain the master ID (security attribute) for an accessing processor wherein a master ID data structure 24 comprises a master ID table (table directory) and a lookup table (security attribute table) (column 6,lines 48-54).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) patent may not be obtained though the invention is not identically disclose or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 10, 20, 22, 26, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mamyama (6,052,763) in view of applicant's admitted prior art.

Regarding Claims 10, 22, 26 and 35

Maruyama teaches the memory management system of claims 1, 13, and 23. Maruyama does not teach security attributes comprising a user/supervisor (U/S) bit and a read/write (R/W) bit. Applicant's admitted prior art discloses the memory protection features of an user/supervisor

(U/S) bit and a read/write (R/W) bit where U/S=0 indicates that the memory page is an operating system page, U/S=1 indicates that the memory page is an user memory page, R/W=0 indicates that only read accesses are allowed, and R/W=1 indicates that both read and write accesses are allowed to the memory page (Page 5, lines 4-18). Therefor It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the protection features disclosed in applicant's admitted prior art to the memory management system of Maruyama. This would have been obvious because person having ordinary skill in the art at the time the invention was made would have been motivated to do so since these features would add further security to the system by allowing the further access controls such as user or supervisor assigned memory areas and memory areas assigned as read-only or read-write areas.

Regarding Claim 20

Maruyama teaches the memory management system of claim 13. Maruyama does not teach a physical address within a selected memory page including a base address and an offset. Applicant's admitted prior art teaches a lower portion of an address (offset) being used as an index of the memory page and a page frame base address being used to select the corresponding memory page. When the offset and the base address are combined, they form a physical address (Page 4, lines 21-25).

Therefore It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Maruyama's system to include a physical address within a selected memory page including a base address and an offset. This would have been obvious because person having ordinary skill in the art at the time the invention was made would have been motivated to do so in order to give the system the ability to produce a physical address from the input of a linear address since such ability would allow the system in the case where linear addresses are being inputted.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

A.A

Ali Abyaneh
Patent Examiner
Art Unit 2137
11-08-05

EMMANUEL L. MOISE
SUPERVISORY PATENT EXAMINER